Ultra-Low Power Design – Charge Recycling by Voltage Stacking

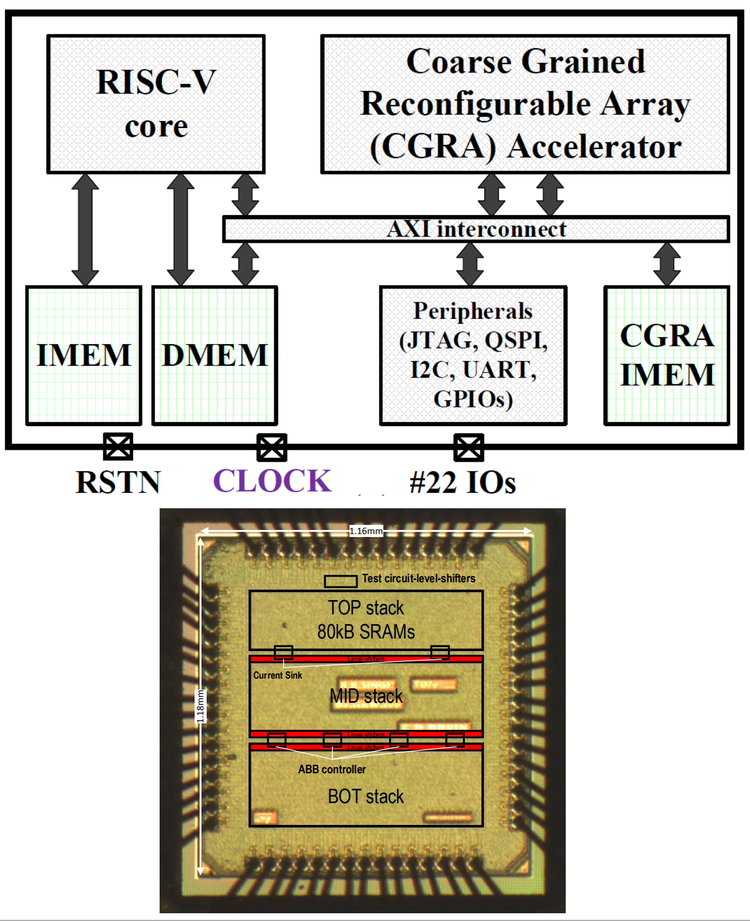
Kamlesh Singh

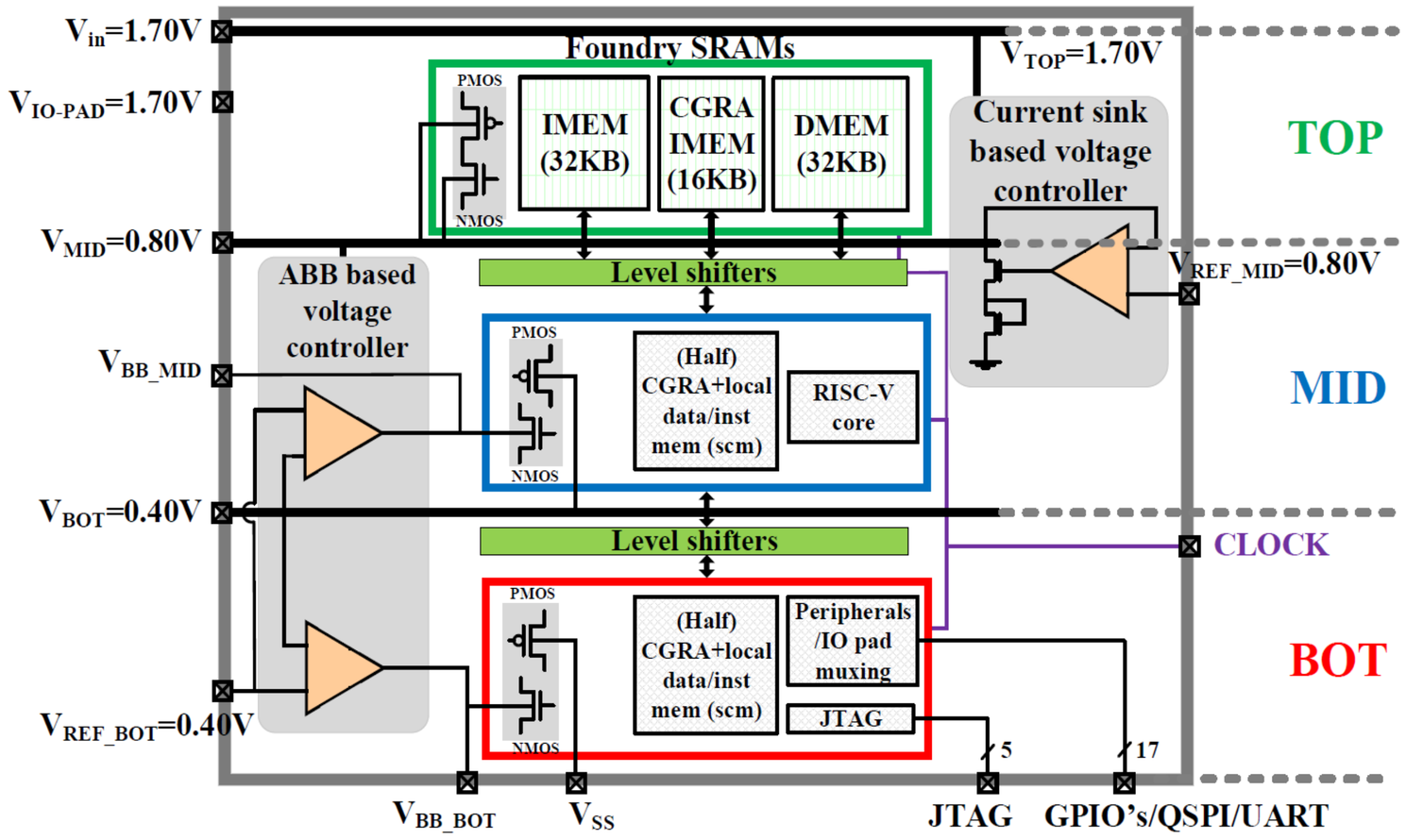
Supervisors: prof. dr. José Pineda de Gyvez, prof. dr. Henk Corporaal

Voltage-stacking

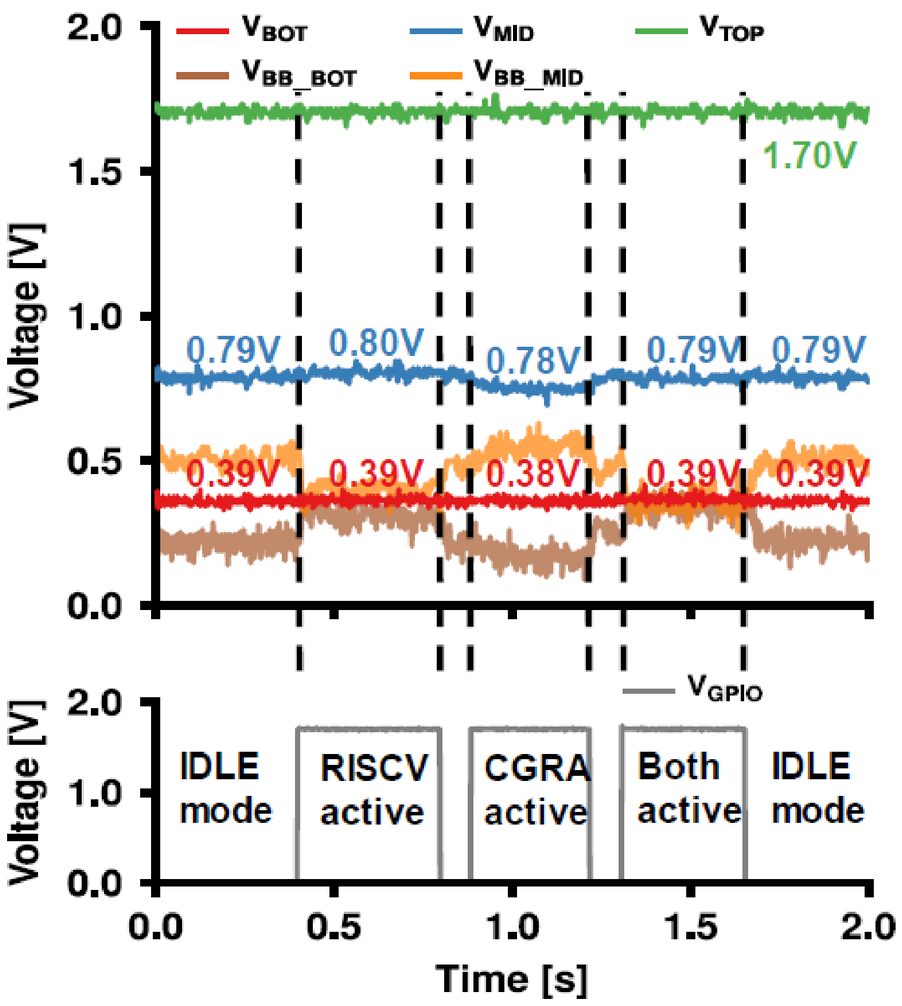
- Voltage scaling to near/sub-threshold voltage to minimize energy consumption
- Charge recycling by stacking the power domains in series instead of parallel
  - ~30% power savings, 95% power delivery efficiency with negligible area overhead
- Current sink-based controllers are used to control the voltage rail between top and middle stacks
- Adaptive body bias controllers are used to control the voltage rail between middle and bottom stacks

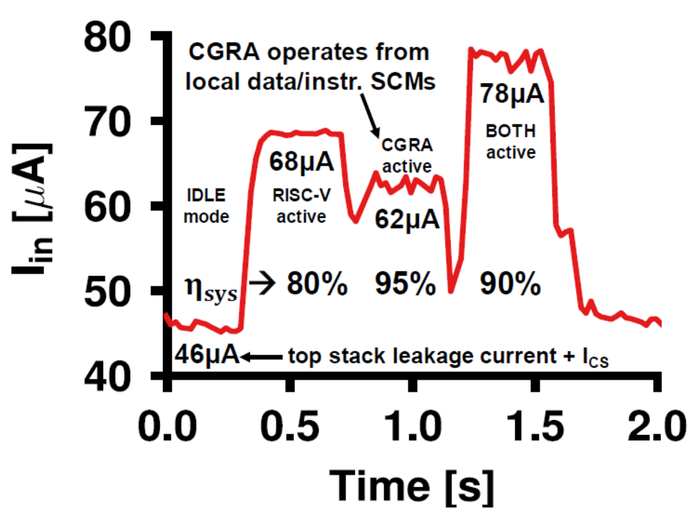
Chip architecture

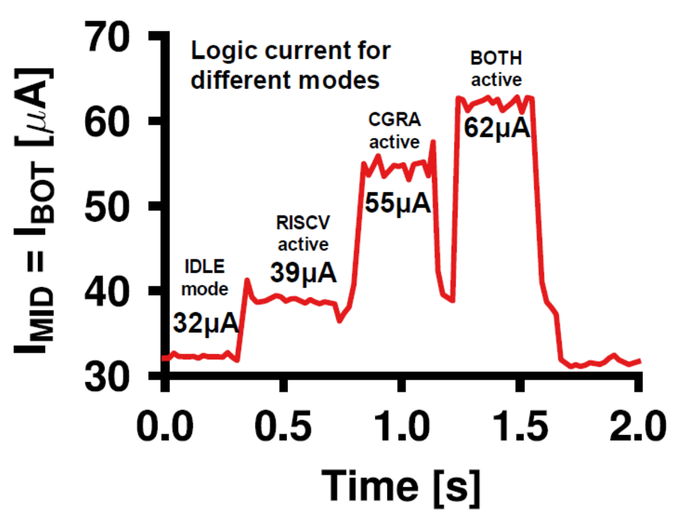




Measurement results







Stacked Mode				Flat mode		
Application	Frequency	Energy/cycle	Energy efficiency	Frequency	Energy/cycle	Energy efficiency
MatMul	**2.8 MHz**	**39.2 pJ/Cycle**	**35.2 MMACs/mW**	**3.0 MHz**	**67.5 pJ/Cycle**	**20.5 MMACs/mW**
Butterworth filtering	**2.8 MHz**	**42.5 pJ/Cycle**	**31.7 MMACs/mW**	**3.0 MHz**	**68.9 pJ/Cycle**	**19.5 MMACs/mW**
Sorting	**2.8 MHz**	**34.0 pJ/Cycle**	**4.6 MCMPs/mW**	**3.0 MHz**	**48.8 pJ/Cycle**	**3.2 MCMPs/mW**